

# **Enhanced 130 nm Generation Logic Technology Featuring 60 nm Transistors Optimized for High Performance and Low Power at 0.7 - 1.4 V**

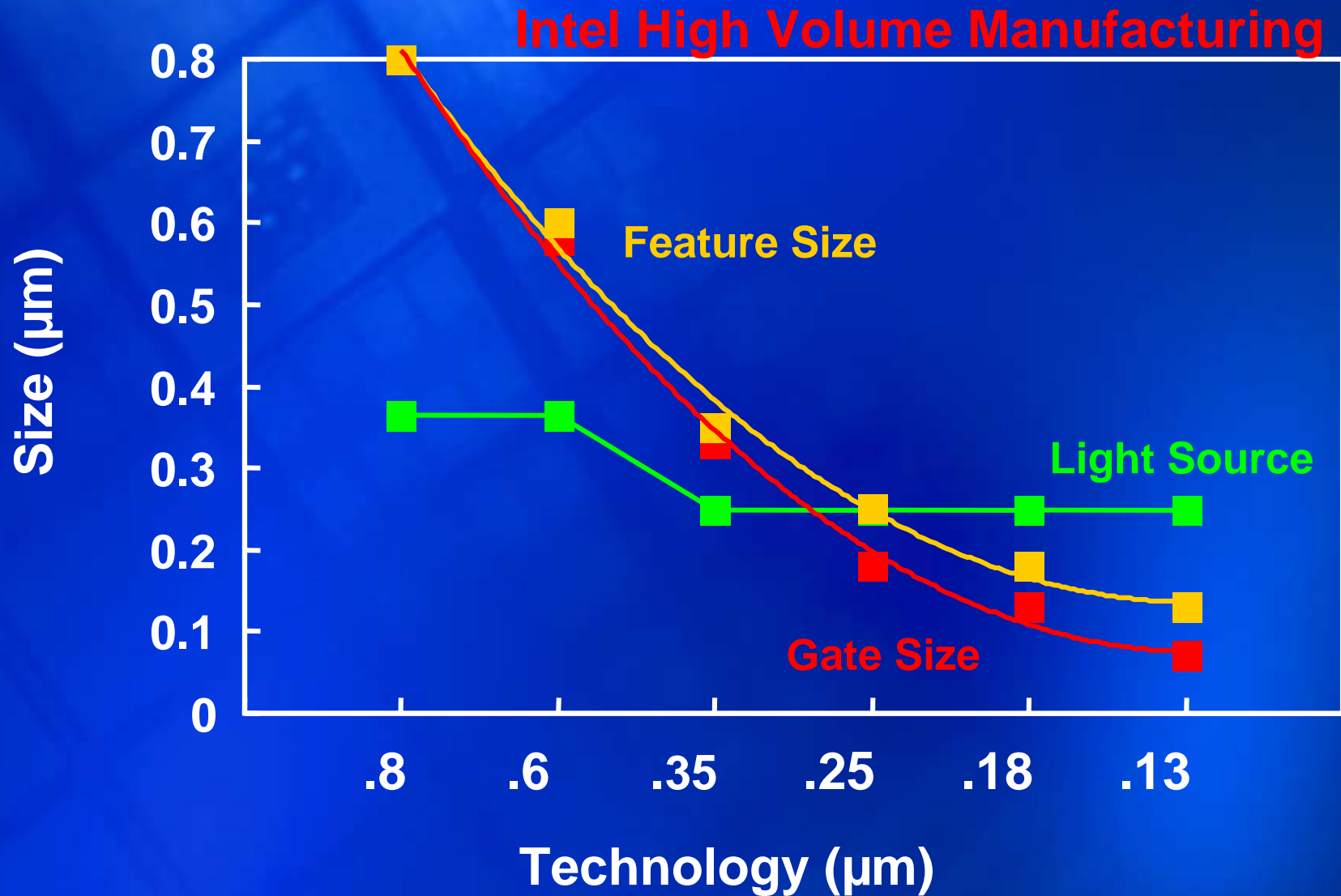
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B. Crew, V. Dubin, M. Hussein, P. Jacob, C. Kenyon, E. Lee<sup>1</sup>, B. McIntyre, Z. Ma,  
P. Moon, P. Nguyen, M. Prince, R. Schweinfurth, S. Sivakumar, P. Smith, M.  
Stettler\*, S. Tyagi, M. Wei<sup>1</sup>, J. Xu, S. Yang and M. Bohr**

**Portland Technology Development, \* TCAD, <sup>#</sup> QRE, <sup>1</sup>CTM, Intel  
Corporation, Hillsboro, OR 97124, USA.**

# Outline

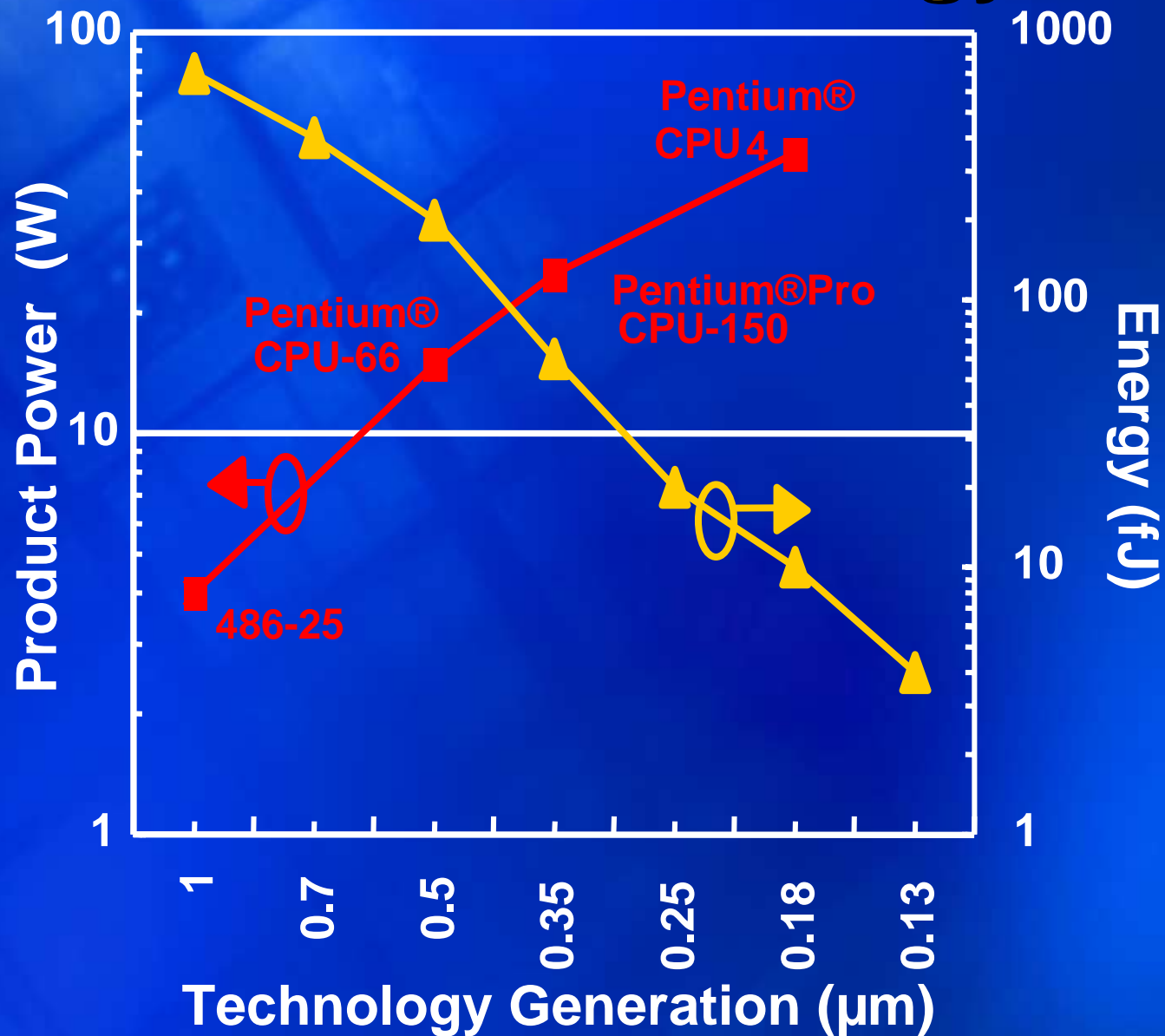
- Introduction
- Process Flow and Technology Features
- Enhanced Transistor Features
  - 1.5 nm  $T_{ox}$  with improved oxide TTF
  - 60 nm transistors
  - Low DIBL
  - Process changes to support 0.7 to 1.4 V operation
- Product Performance
- Conclusions

# Transistor Gate Scaling Trend



- Gate CD in production ~60 nm for 130 nm node

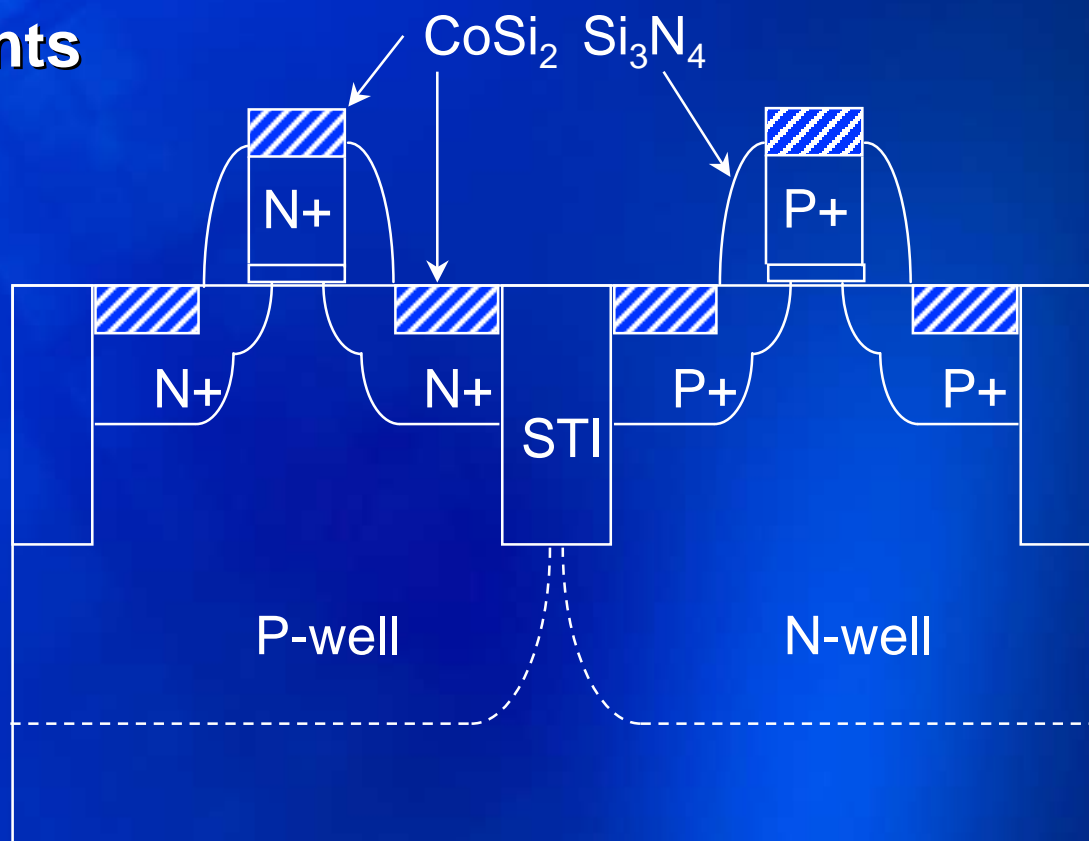
# Product Power and Energy Trends



- Voltage scaling needed to control power

# Front End Process Flow and Features

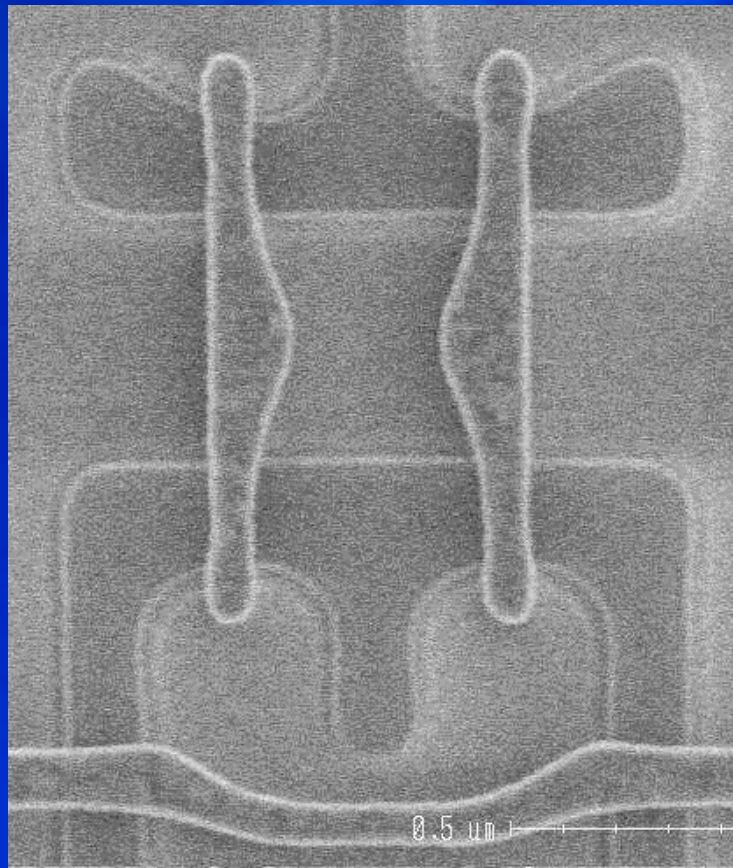
- Shallow Trench Isolation
- Well &  $V_T$  Adjust Implants
- Gate Oxide Formation
- Poly Gate Patterning
- Shallow Source Drain Extensions
- Halo Implants
- $\text{Si}_3\text{N}_4$  Spacer
- Deep Source/Drain
- Co Salicide



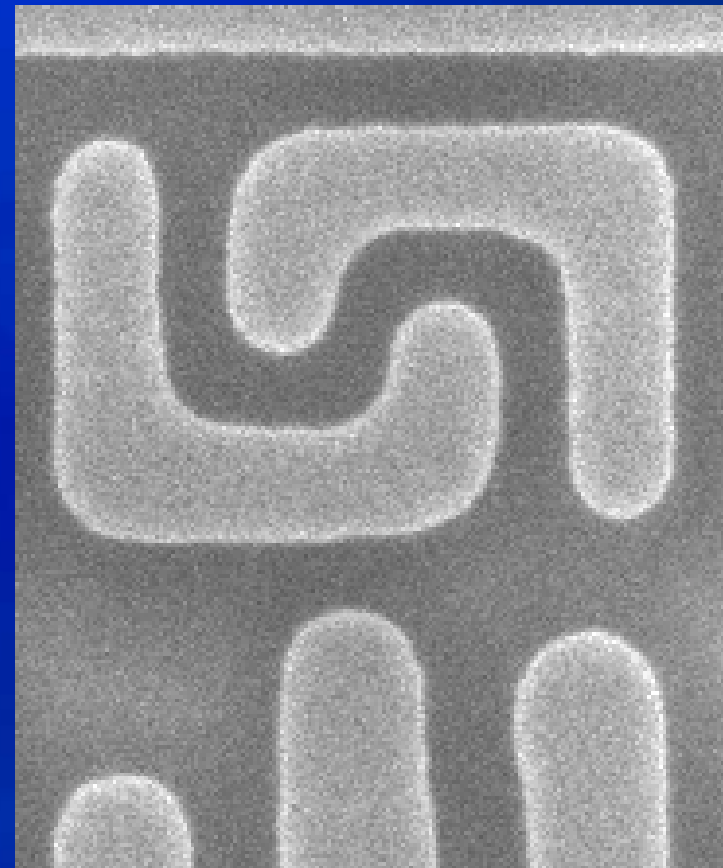


# 2.0 $\mu\text{m}^2$ 6-T SRAM Cell

- Printed with 248 nm lithography



**Poly over STI**



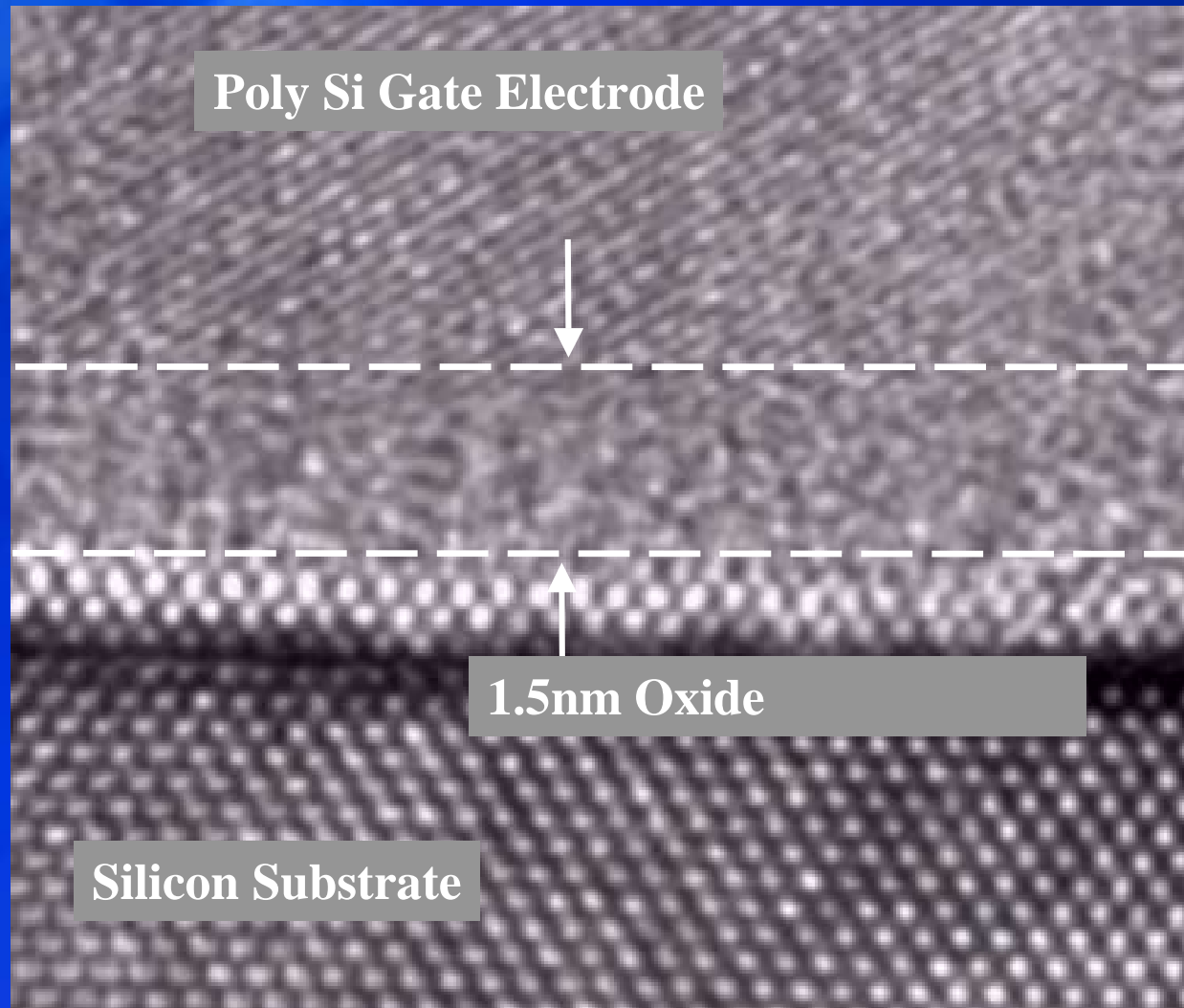
**Metal 1**

$$1.22 \mu\text{m} \times 1.64 \mu\text{m} = 2.0 \mu\text{m}^2$$

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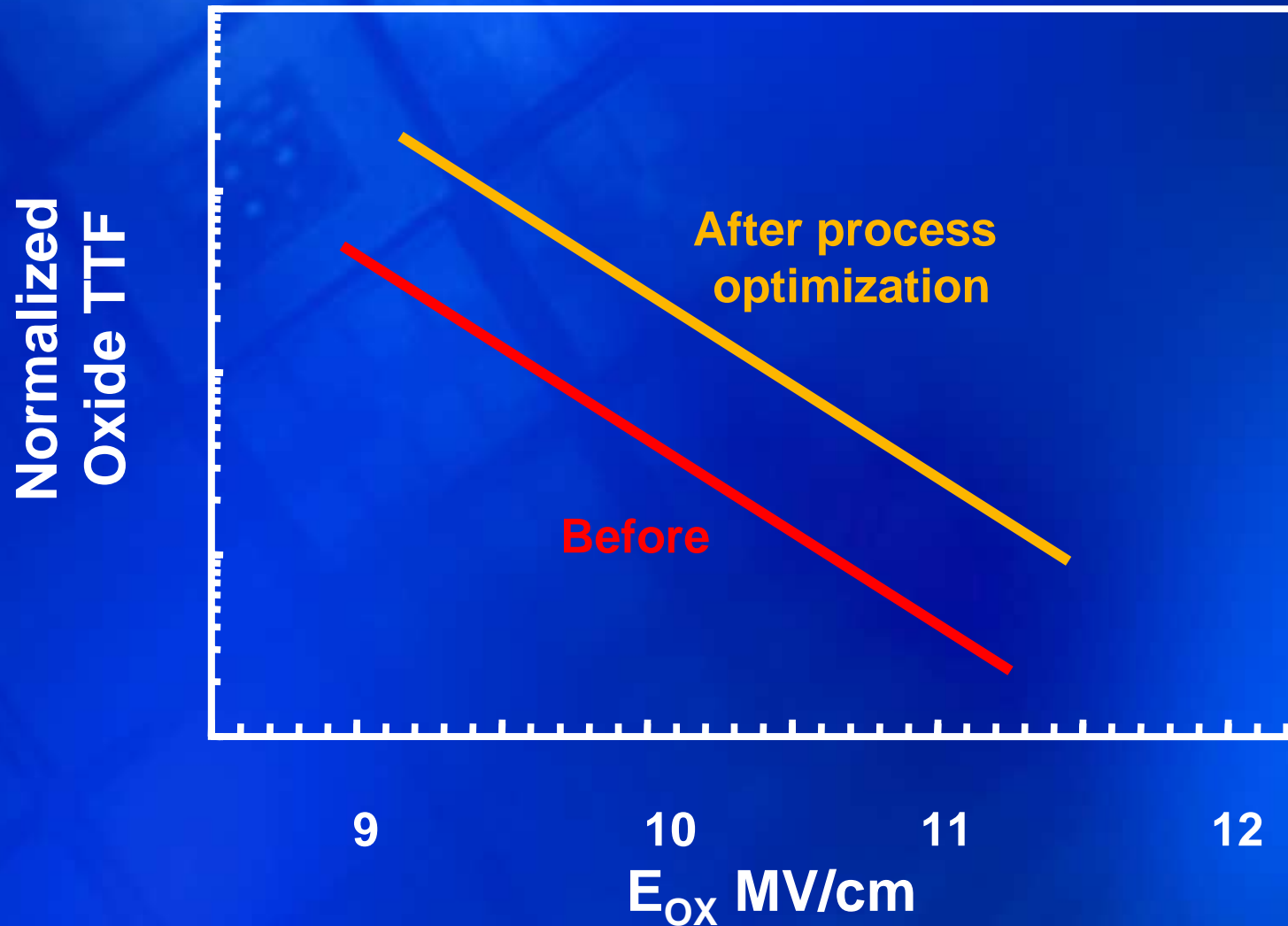
# 1.5nm Electrical $T_{ox}$



- Changes from Intel IEDM 2000 to support 10% higher  $E_{ox}$

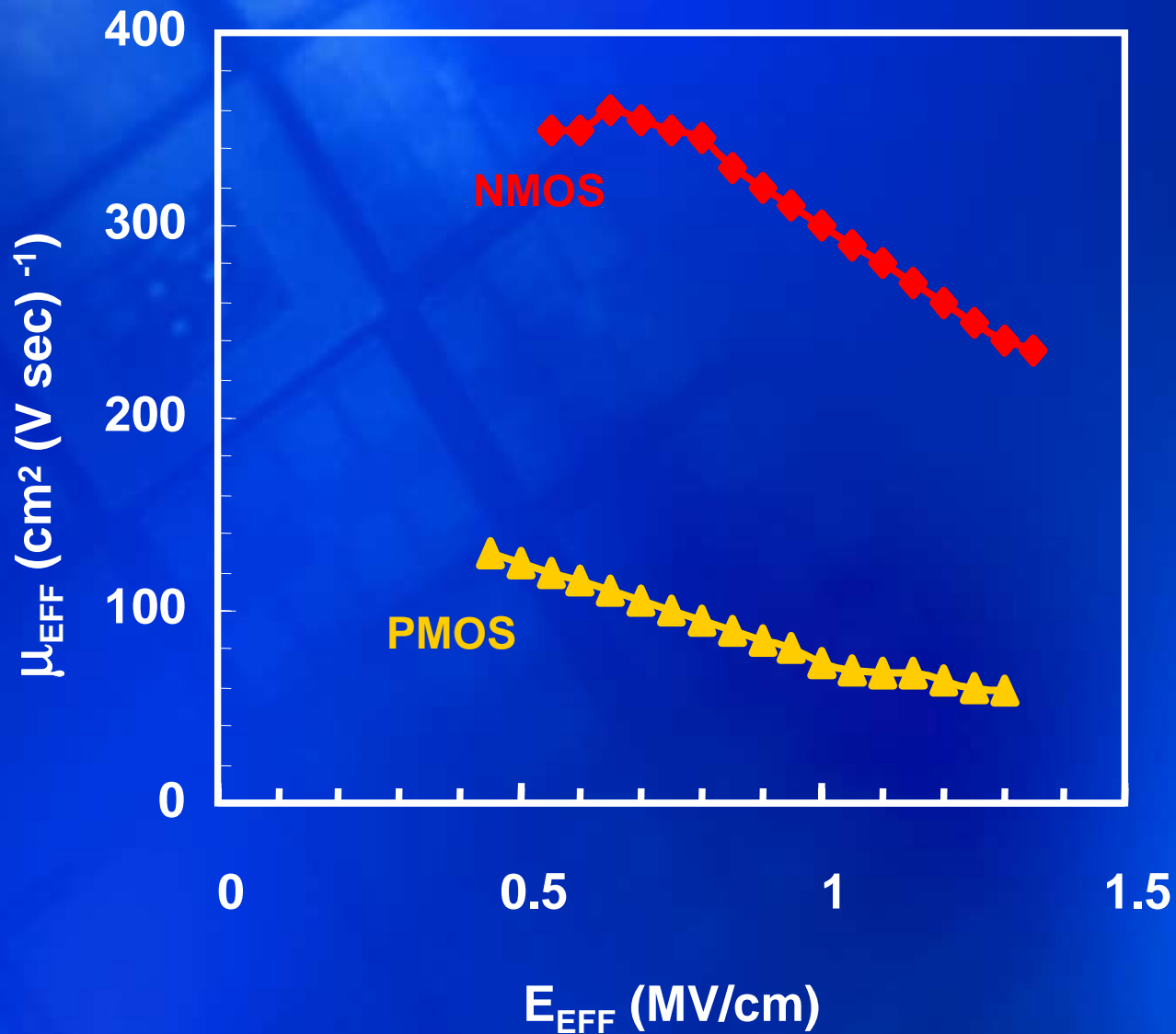


# Improved Oxide Time to Fail



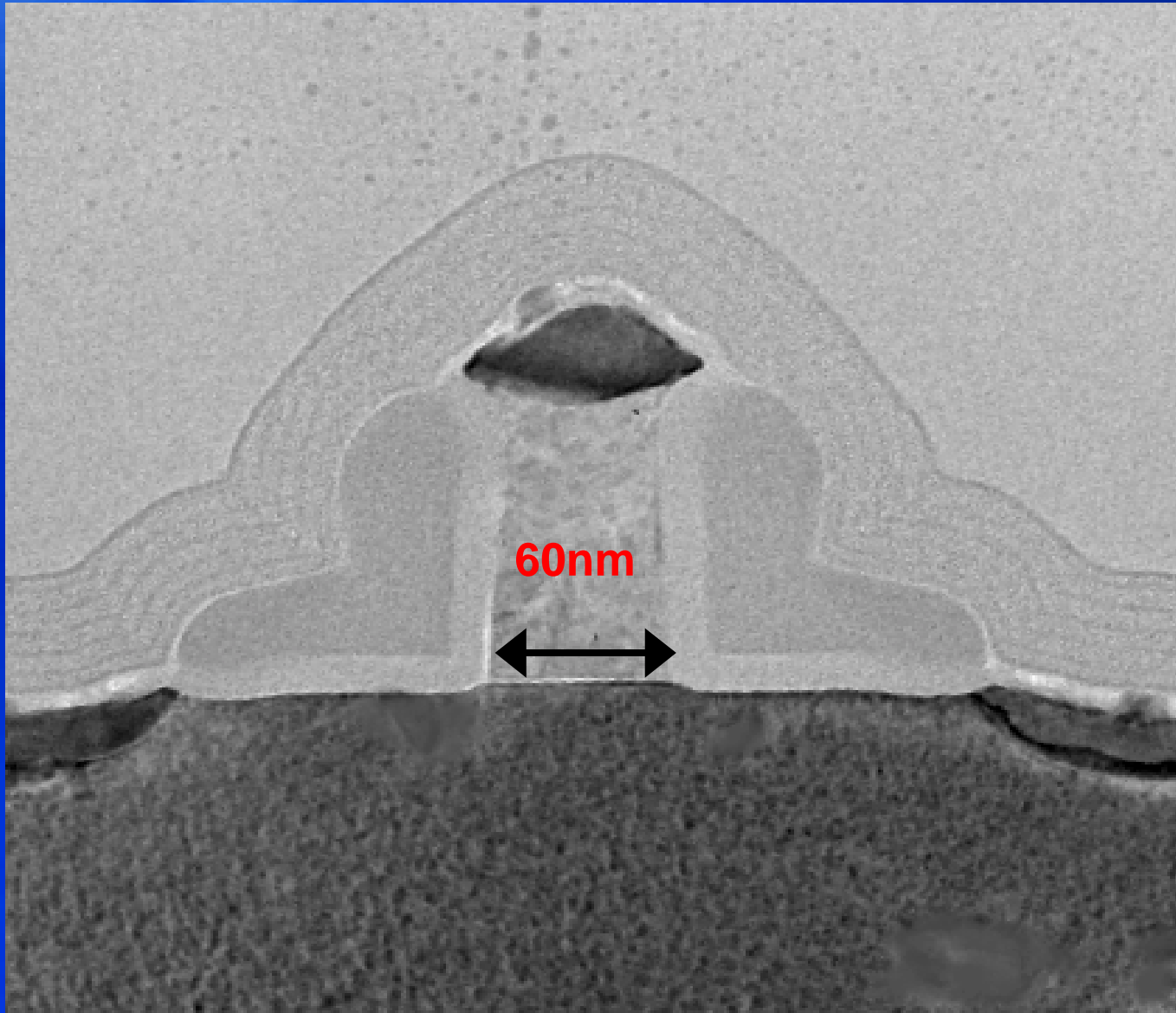
- Same TTF: 10% higher oxide electric field

# High Channel Mobility



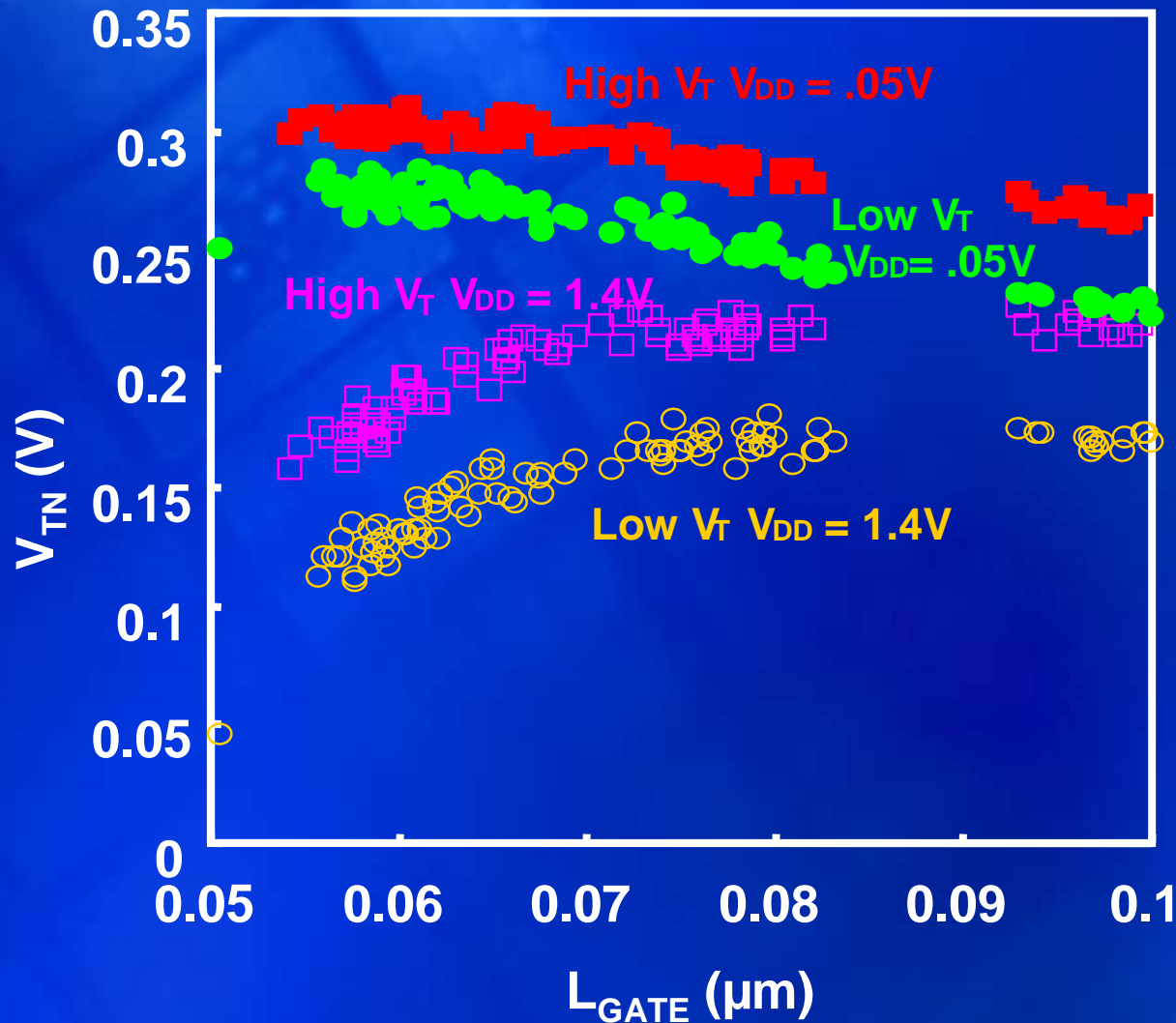
- Mobility improved over Intel IEDM 2000 for high drive current

# 60 nm Nominal Physical Gate Length



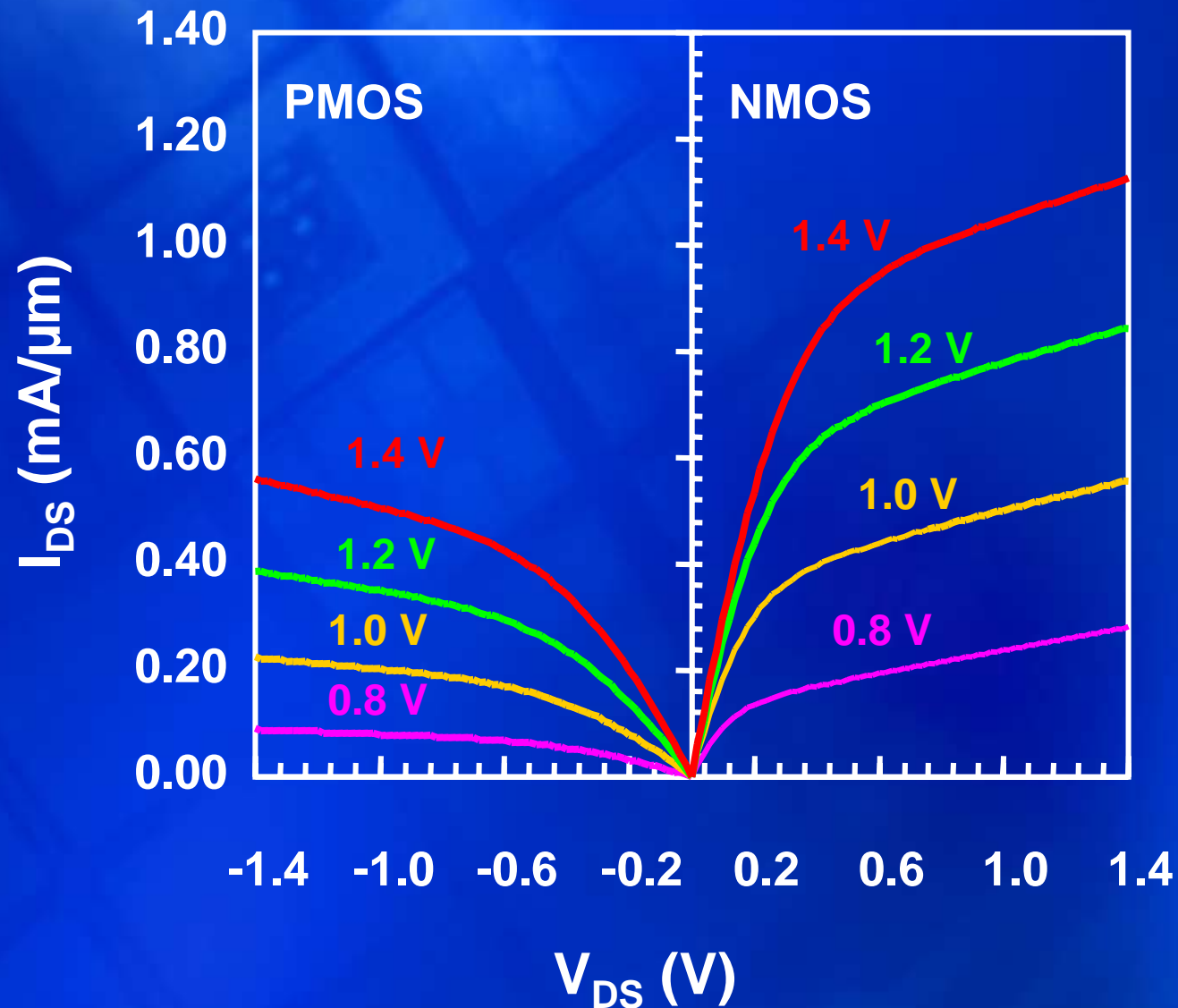
- Nominal  $L_{\text{GATE}} = 60\text{nm}$      $L_{\text{MIN}} = 60\text{nm}$  – CD control

# Excellent Short Channel Effects (Low DIBL)



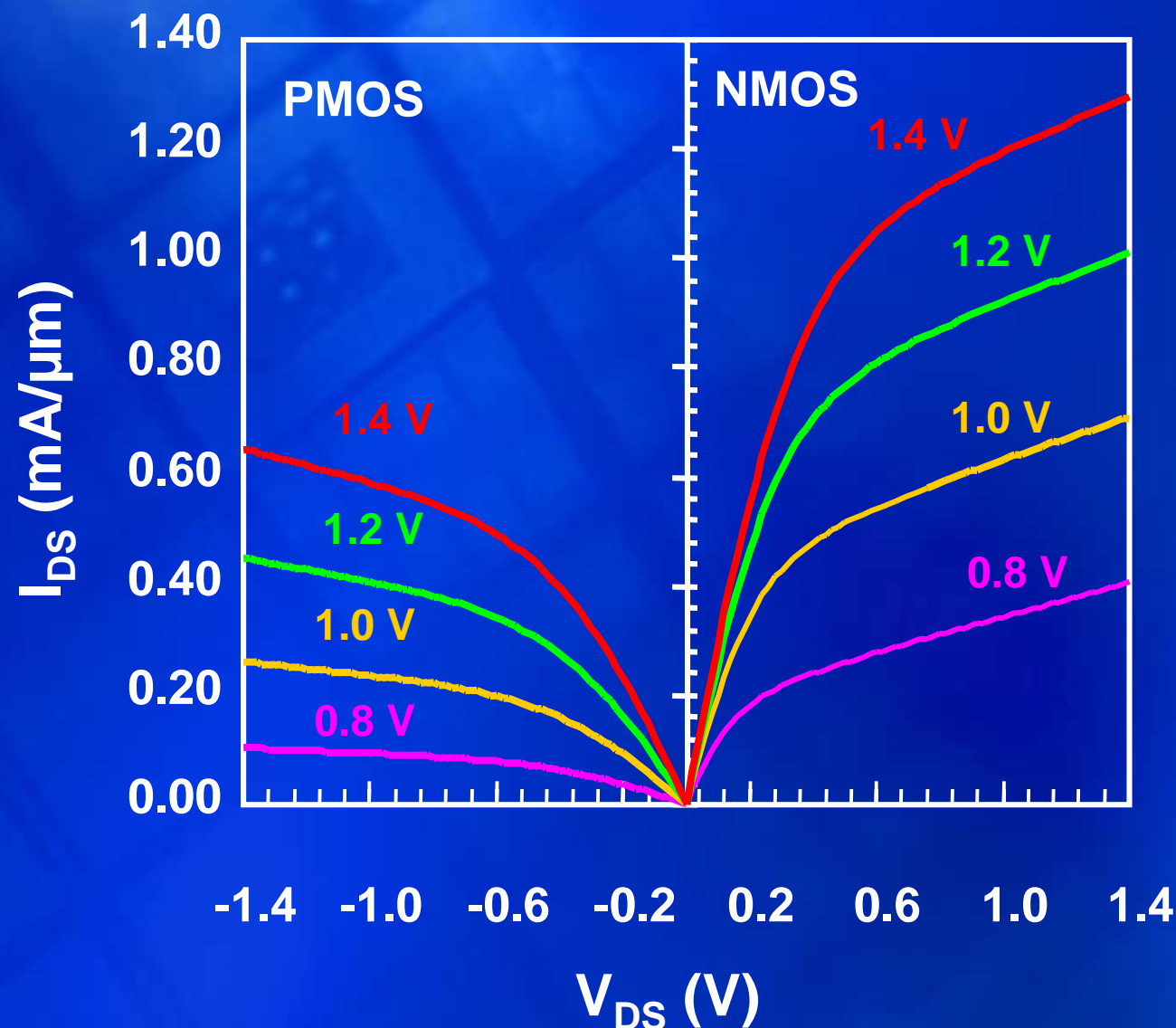
- Low DIBL < 100mV / V
- Key to high product performance

# High $V_T$ Device: $I_D - V_D$ Curves



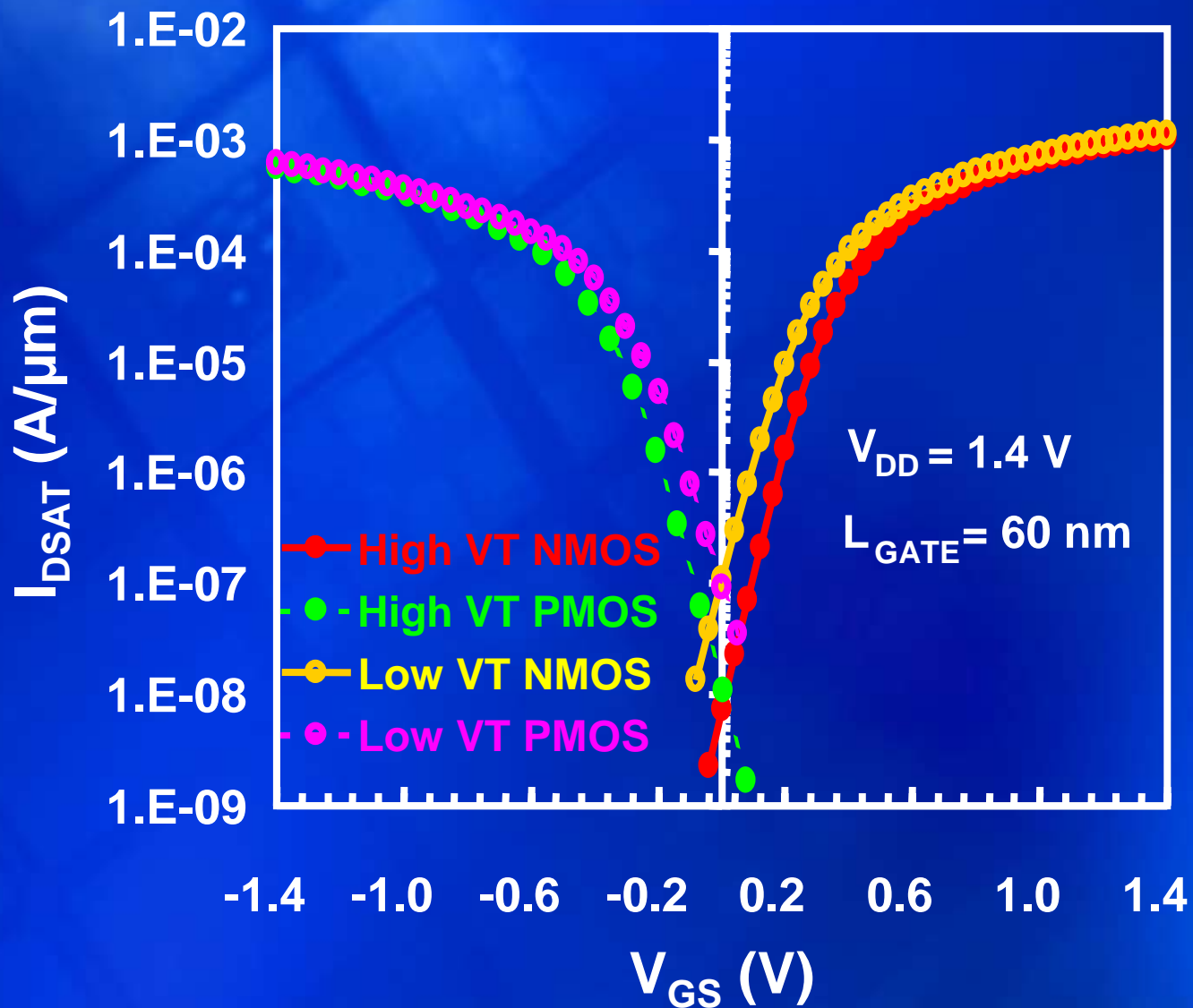
- 1.14  $\text{mA}/\mu\text{m}$  NMOS
- 0.56  $\text{mA}/\mu\text{m}$  PMOS

# Low $V_T$ Device: $I_D - V_D$ Curves



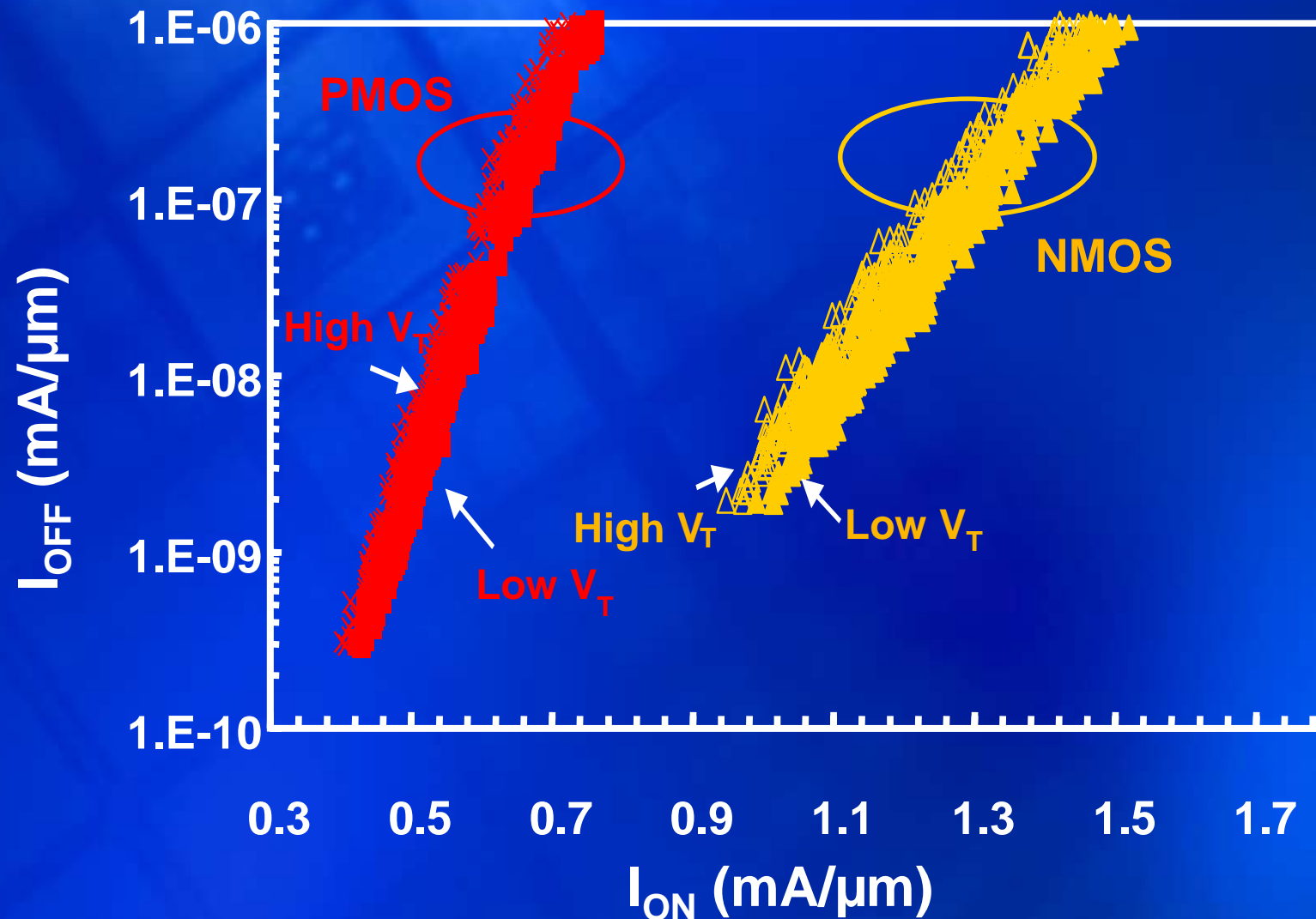


# Sub-Threshold Slope



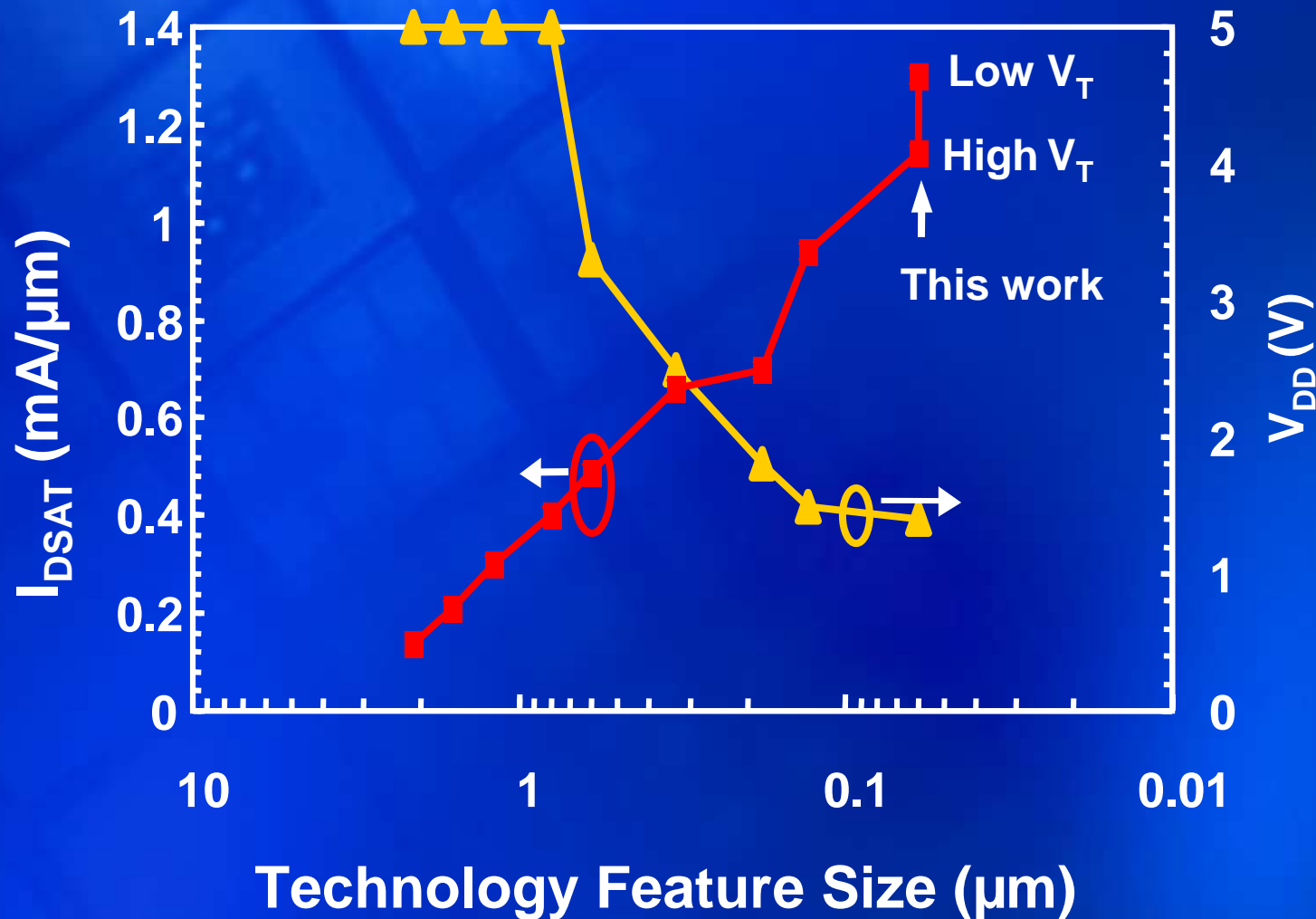
- Well controlled  $\sim 80$  mV sub-threshold slope

# $I_{ON}$ vs $I_{OFF}$



- Same  $I_{ON}$  vs  $I_{OFF}$  for low and high  $V_T$  devices

# Intel NMOS Drive Current Trend

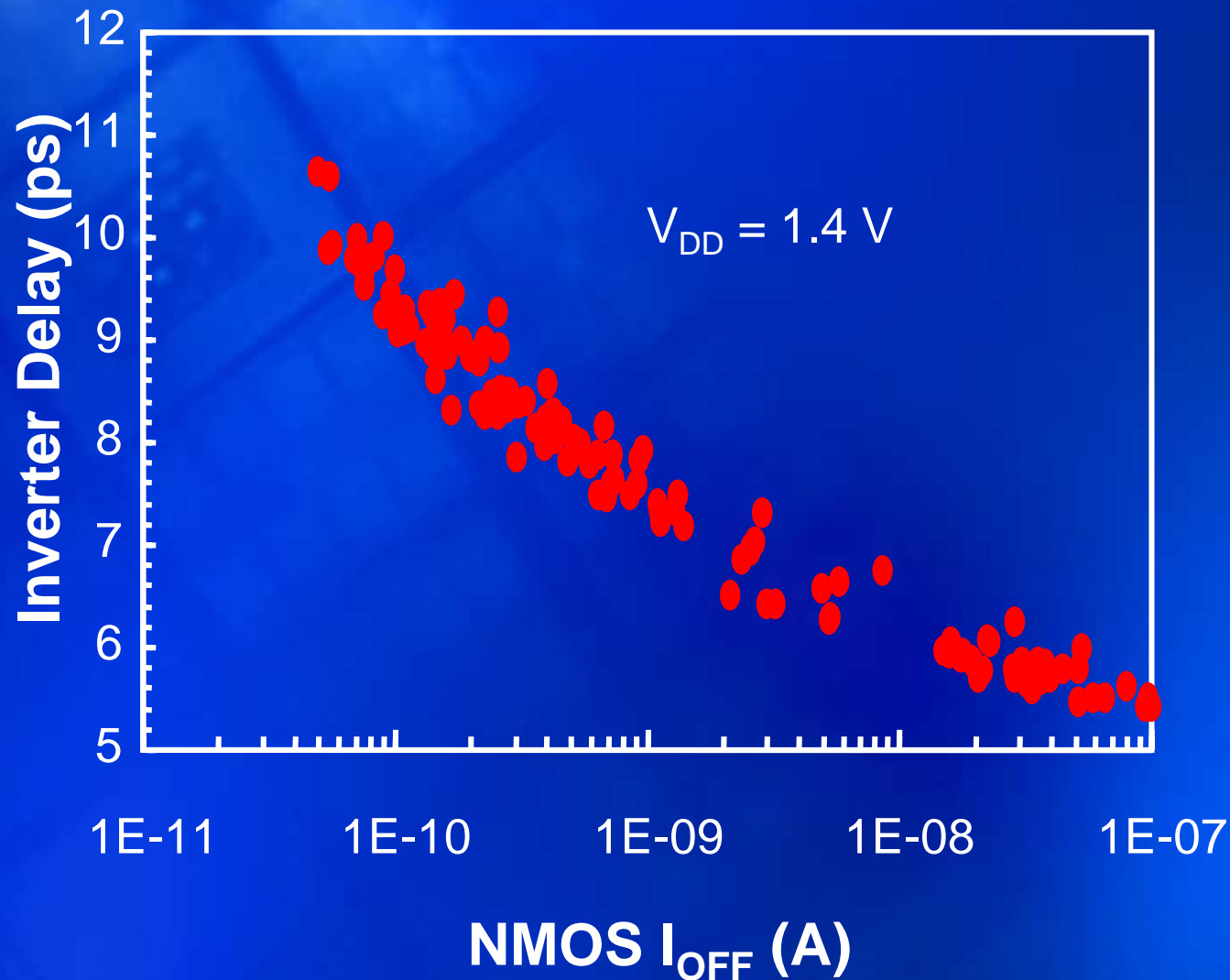


- Continues trend of higher drive current with each technology node

# Outline

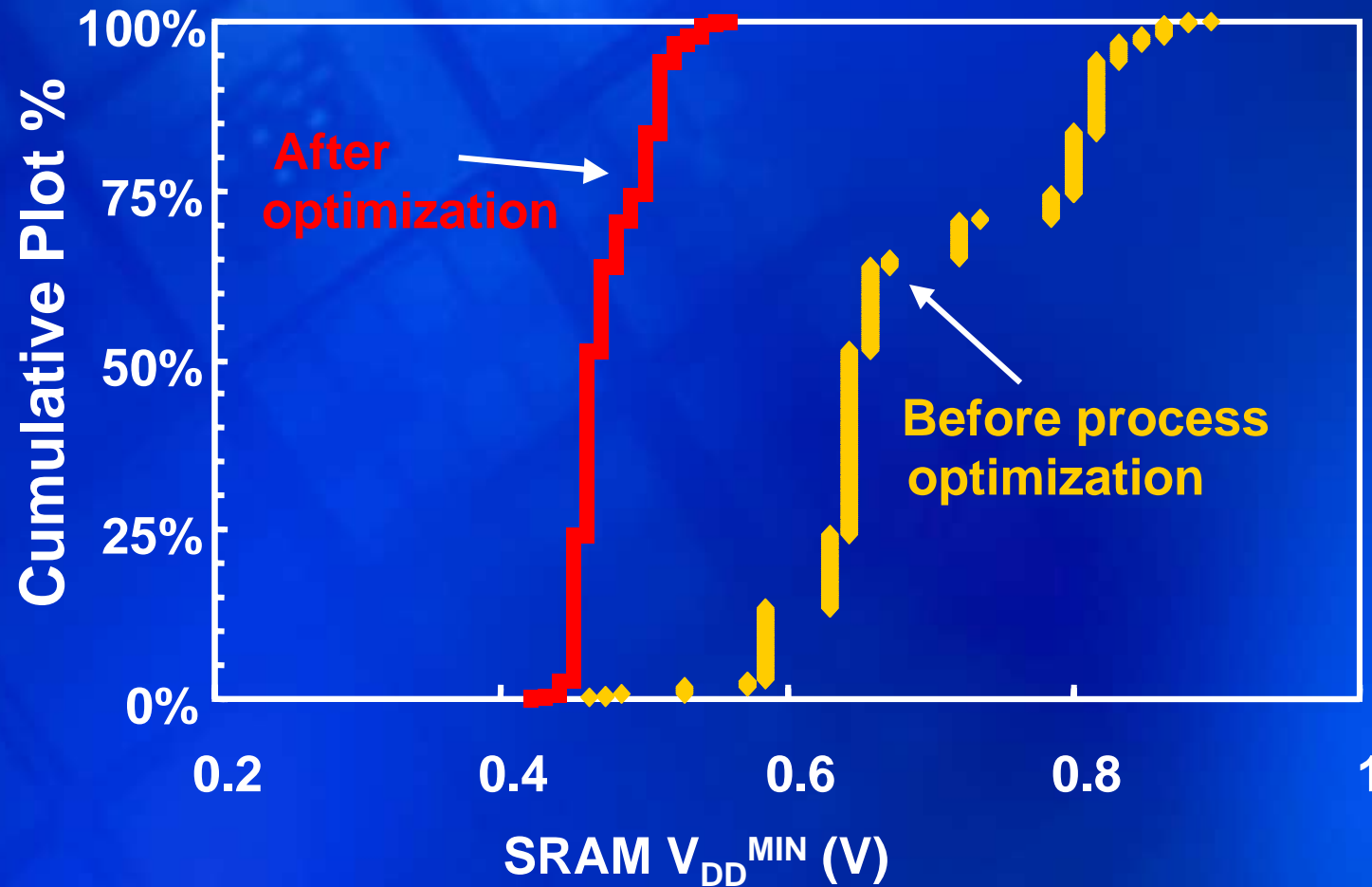
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# Inverter Delay



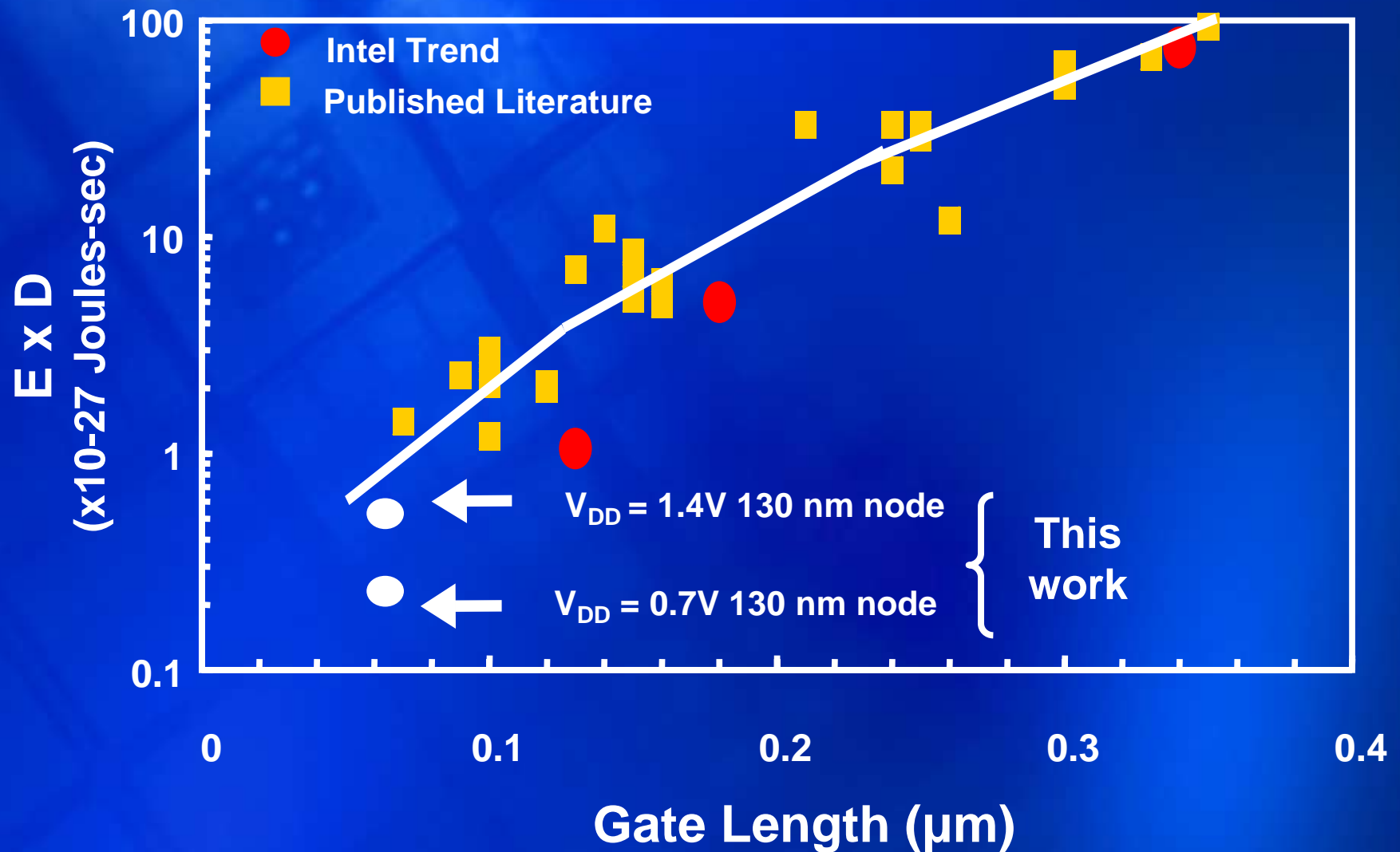
- 6.5 ps delay for  $I_{OFF} = 10 \text{ nA}/\mu\text{m}$
- 5.5 ps delay for  $I_{OFF} = 100 \text{ nA}/\mu\text{m}$

# Low Voltage Operation





# Leading Energy X Delay

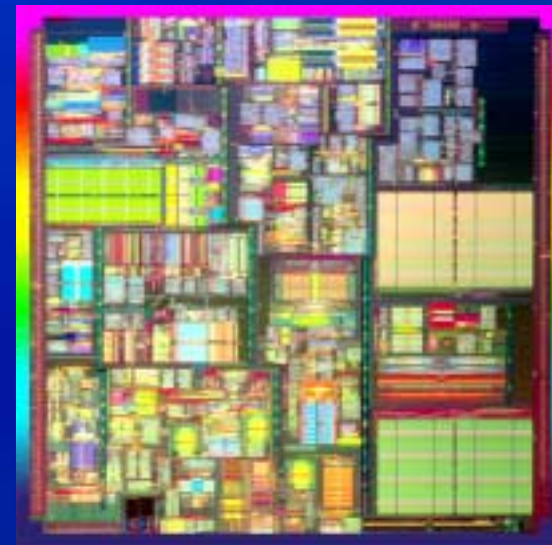


- Industry leading energy delay product

# Product Performance: Pentium®IV Microprocessors

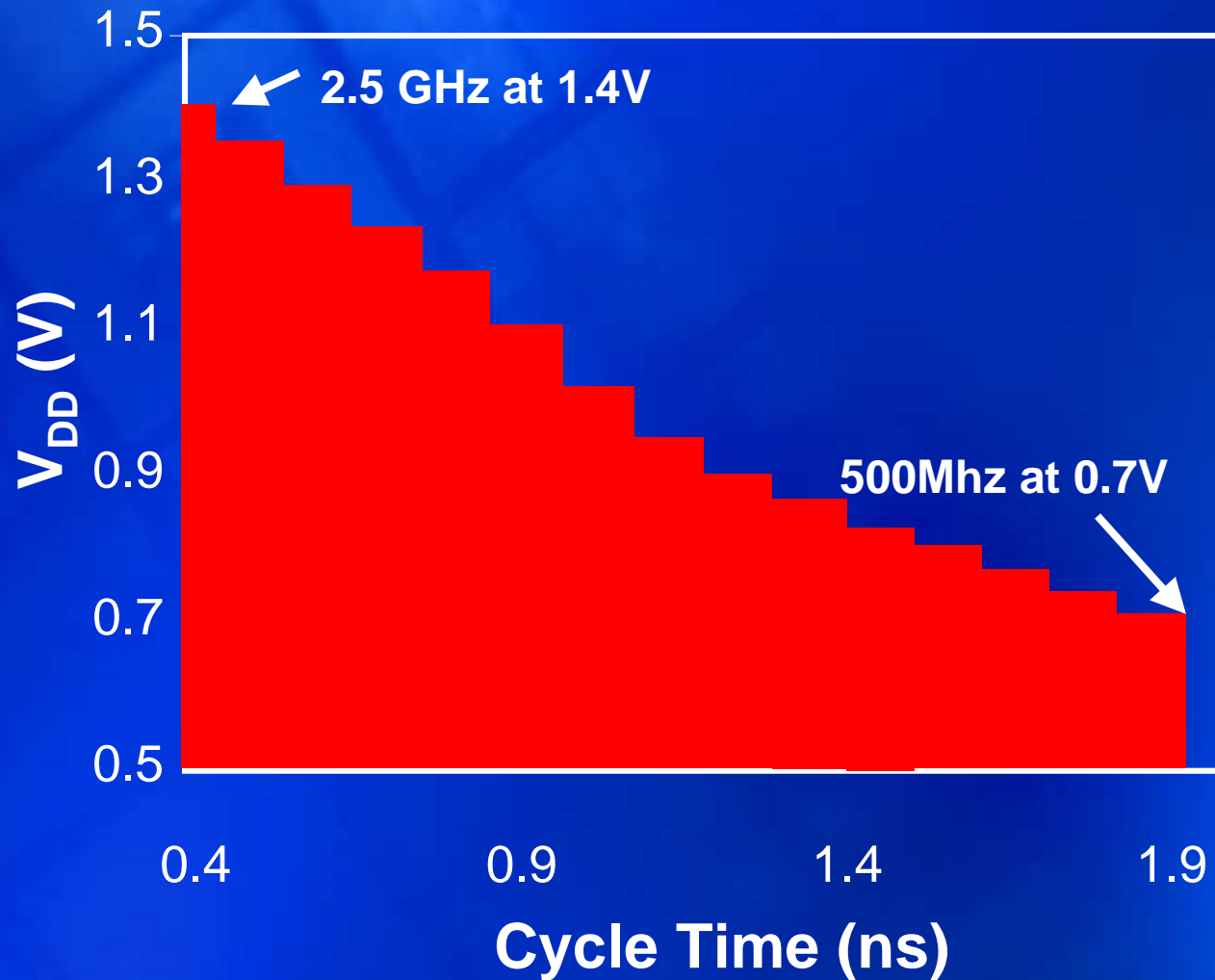


**180 nm Technology**



**130 nm Technology**

# Pentium® IV Microprocessors Schmoos Plot



- Up to 2.5 Ghz operation

# Conclusions

- 60 nm transistors with NMOS drive current of 1.3 mA/ $\mu$ m achieved
- Low DIBL at  $< 100$  mV / V
- Enhancements to process technology allows for 0.7 to 1.4 V operation
- Excellent integrated performance demonstrated
  - 5.5 to 6.5 ps inverter delay
  - 2.5 GHz operation

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- Quality and Reliability Engineering
- Technology Computer Aided Design



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